



EL979950106

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/875,501
Filing Date June 4, 2001
Inventor Klaus F. Schuegraf, et al.
Assignee Micron Technology, Inc.
Group Art Unit 2815
Examiner E. Ortiz
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, a copy of which is attached. No admission is made regarding whether all the submitted references are prior art.

Citation of these references is respectfully requested.

Respectfully submitted,

RECEIVED
DEC 24 2003
TC 2800 MAIL ROOM

Dated:

12-12-03

By:

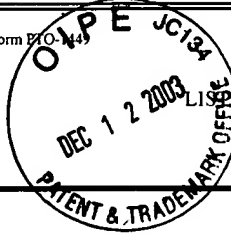


D. Brent Kenady
Reg. No. 40,045

12/17/2003 MAHHE1 00000079 09875501

02 FC:1806

180.00 OP

Form PTO-14		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1741		SERIAL NO. 09/875,501	
 LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Klaus Florian Schuegraf et al.			
				FILING DATE 06/04/01		GROUP 2815	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AC			Ohnishi, K. et al., <i>Improving Gate Oxide Integrity (GOI) of a W/Wnx/dual-poly Si Stacked-Gate by Using Wet-Hydrogen Oxidation in 0.14-μm CMOS Devices</i> . IEEE. 1998. pgs. 397-400.			
	AD			Kawada, K. et al., <i>Water Vapor Generator By Catalytic Reactor</i> , pgs. 10-16.			
	AE			Wakabayashi, H. et al., <i>An Ultra-Low Resistance and Thermal Stable W/pn-Poly-Si Gate CMOS Technology using Si/TiN Buffer Layer</i> . IEEE. 1998. pgs. 393-396.			
	AF			Hiura, Y. et al., <i>Integration Technology of Polymetal (W/WSiN/Poly-Si) Dual Gate CMOS for 1 Gbit DRAMs and Beyond</i> . IEEE. 1998. pgs. 389-392.			
	AG			Nagahama, T. et al., <i>Wet Hydrogen Oxidation System for Metal Gate LSI's</i> . pgs. 140-143			
	AH			Lee, B. et al., <i>In-situ Barrier Formation for High Reliable W/barrier/poly-Si Gate Using Denudation of W_{N2} on Polycrystalline Si</i> . IEEE. 1998 pgs. 385-389.			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

RECEIVED
 DEC 24 2003
 TOLSON MAIL ROOM